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JONES & VOLENTINE, L.L.P.
Suite 150
12200 Sunrise Valley Drive
Reston, VA 20191

EXAMINER	
MAI, ANH D	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040107

Application Number: 09/768,271
Filing Date: January 25, 2001
Appellant(s): YAJIMA, TSUKASA

Andrew J. Telesz, Jr.
Reg. No. 33,581
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 5, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 6-9 and 11-19 stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,605,853	Yoo et al.	2-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 6-9 and 11-19 stand are rejected under 35 U.S.C. 102(b) as being anticipated by Yoo et al. (U.S. Patent No. 5,605,853) (of record).

With respect to claim **6**, insofar as the apparatus is concerned, Yoo teaches a semiconductor device as claimed including:

first and second gates (16) formed on an active region of a substrate (10), the first and second gates (16) consisting of a refractory metal layer (28) on a polysilicon layer (16);

a field oxide (12) formed on the substrate (10) between the first and second gates (16);

side walls (20) formed on side surfaces of the gates (16), the side walls (20) being a silicon oxide film;

a protective layer (21) formed selectively on the field oxide (12), the protective layer (21) being a material (polysilicon) different than the field oxide (silicon oxide); and

an insulating layer (38) , a contact hole and a connecting wire (40) formed above a surface of the substrate (10). (See Fig. 7, col. 3-5).

Product by process limitation:

The expression "to prevent overetching of said field oxide" (claims 6, 11 and 16) is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. The same reasoning also applies to claims 11 and 16.

In any event, since the protective layer (21) of Yoo is formed on the field oxide (12) and is made of a material different than the field oxide, the protective layer (21) functions to prevent overetching of the field oxide as well. Therefore, the protective layer (21) of Yoo appears to meet the process limitation "to prevent overetching of said field oxide" recited in the present claims.

With respect to claim **11**, insofar as the apparatus is concerned, Yoo teaches a semiconductor device as claimed including:

a gate (16) formed on an active region of a substrate (10);

a field oxide (12) formed on the substrate adjacent the active region;

a protective layer (21) formed on the field oxide (12), the protective layer (21) being a material (polysilicon) different than the field oxide (silicon oxide); and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above a surface of the substrate (10),

the protective layer (21) being formed on the field oxide (12) only. (See Fig. 7, col. 3-5).

With respect to the Product-by-Process limitation the explanation provided above for the protective layer (21)of Yoo, applies to claim 11 as well.

With respect to claim **16**, insofar as the apparatus is concerned, Yoo teaches a semiconductor device as claimed including:

a gate (16) formed on an active region of a substrate (10), the gate (16) consisting of a refractory metal layer (28) on a polysilicon layer (16);

side walls (20) formed on side surfaces of the gates (16), the side walls being a silicon oxide film;

a field oxide (12) formed on the substrate (10) adjacent the active region;

a protective layer (21) formed on the field oxide (12), the protective layer being a material (polysilicon) different than the field oxide (silicon oxide); and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above a surface of the substrate (10),

the protective layer (21) being formed on the field oxide (12) only (See Fig. 7, col. 3-5).

With respect to the Product-by-Process limitation the explanation provided above for the protective layer (21)of Yoo, applies to claim 16 as well.

With respect to claims 7, 12, 17, the protective layer (21) is a polysilicon layer.

With respect to claim 8, the protective layer (21) of Yoo is formed on the field oxide (21) only.

With respect to claims 9, 13, 18, the gate (16) is a MOSFET gate.

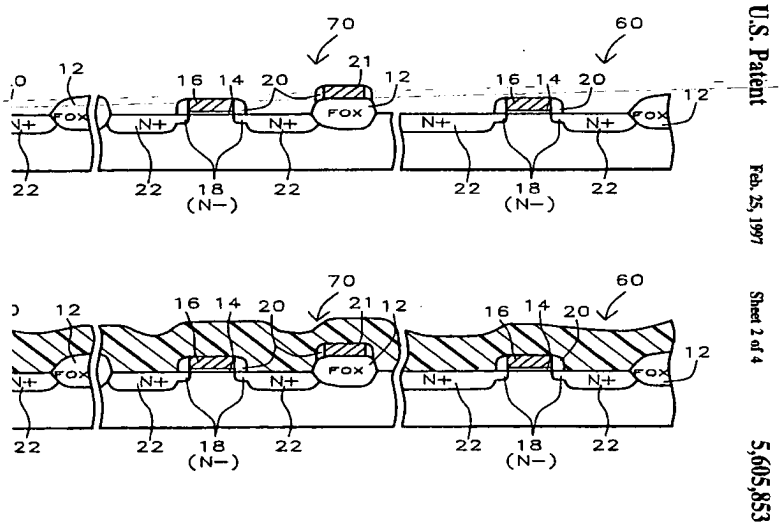
With respect to claim 14, the gate (16) of Yoo further comprises side walls (20) formed on side surface of the gate (16), the side walls being covered by the insulating layer (38).

With respect to claims 15, 19, the semiconductor device of Yoo further comprises an additional gate (16) formed on the substrate (10), the field oxide (12) is formed on the substrate between the gate (16) and the additional gate (16).

(11) Response to Argument

Appellant argues that layer (21) in Figs. 2-7 of the Yoo et al. reference cannot be interpreted as the protective layer as specified in claim 6, because layer (21) cannot be formed on field oxide (FOX) layer (12) (as would be necessary to meet the features of claim 6) and function as a working floating gate.

Contrary to the assertion, layer (21) of Yoo meets the limitation as recited in claim 6 including: formed on the field oxide (12) and being a material (polysilicon) different than the field oxide (silicon oxide). (See Fig. 2 and col. 3, line 64-col. 4, line 8). Since layer (21) is formed on the field oxide layer 12, as seen in the figure from Yoo reproduced below, and since layer 21 is of a material different from layer 12, one of ordinary skill would readily conclude that layer 21 protects layer 12.



U.S. Patent Feb. 25, 1997 Sheet 2 of 4 5,605,853

In citing publications by Haddad et al. and Wolf and Mizutani (U.S. Patent No. 4,637,128), Appellant appears to contend that layer (21) cannot be formed on field oxide (FOX) layer (12) and the field oxide (FOX) layer (12) must be a thin insulating layer. However, Fig. 2 clearly shows that layer (21) does form on field oxide (12) (which is thick). Whether the field oxide of Yoo is "thick" or "thin" appears to be immaterial to the present claims because the thickness of field oxide has not been specified in the claims. Furthermore, the claims in Yoo specifically state: "forming a floating gate over a field oxide region in said second memory region" (claim 1, col. 6, lines 1-2). Therefore, nothing in the reference cited by the Appellant contradicts the disclosure in Yoo.

Additionally, Appellant emphasizes that layer (21) of Yoo is described in column 3, lines 15-17 as formed **over** a field oxide region, not specifically on a field oxide region.

Drawings are parts of the specification, Fig. 2 in Yoo clearly shows that there is no intervening layer between layer (21) and the field oxide (12). Therefore, one of ordinary skill in the art would readily ascertain that layer (21) is formed **on** or directly **over** the field oxide (12).

It is unequivocal that layer (21) is formed on field oxide (FOX) layer (12). This has been fully disclosed in the specification and also specified in the claims in Yoo. Further, layer (21) is made of a polysilicon material, thus, different than the silicon oxide of the field oxide (12).

Since layer (21) is of a material different than the field oxide (12) and formed on the field oxide (12), the device of Yoo anticipates the claimed device.

With respect to the argument relating to claims 11 and 16, Appellants appear to set forth the same arguments as provided for claim 6. Therefore, the answer provided above applies to claims 11 and 16 as well.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

A.M

January 27, 2004

Conferees
Olik Chaudhuri, SPE W.F. for Olik Chaudhuri
Wael Fahmy, SPE W.F

JONES & VOLENTINE, L.L.P.
Suite 150
12200 Sunrise Valley Drive
Reston, VA 20191